

IN THE DRAWINGS

Proposed changes to Figs. 13 and 14 are submitted herewith,
with a Submission of Proposed Drawing Amendments.

REMARKS

Reconsideration and allowance of this application are respectfully requested in light of the above amendments and the following remarks.

The Applicant acknowledges with appreciation the indication in the Office Action that claims 4-8 are allowed and claims 1-3, 10, and 12 are allowable. Allowable claims 10 and 12 have been rewritten in independent form as new claims 13 and 14 to include the features of their respective base claims and to avoid the issues underlying the applied objections and section 112, second paragraph, rejection. Therefore, allowance of claims 13 and 14 is warranted.

The abstract has been amended to overcome the objection thereto.

Figs. 13 and 14 have been amended to label them as related art and thereby overcome the applied objections.

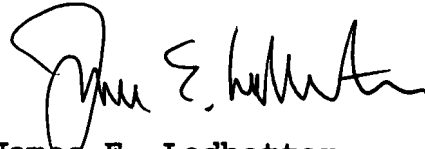
Independent claims 1-4 and 7 have been amended to overcome the applied objections and section 112, second paragraph, rejections. Therefore, allowance of claims 1-3 is warranted.

Claims 9-12 have been canceled.

In view of the above, it is submitted that this application is in condition for allowance, and a notice to that effect is respectfully solicited.

If any issues remain which may best be resolved through a telephone communication, the Examiner is requested to telephone the undersigned at the local Washington, D.C. telephone number listed below.

Respectfully submitted,



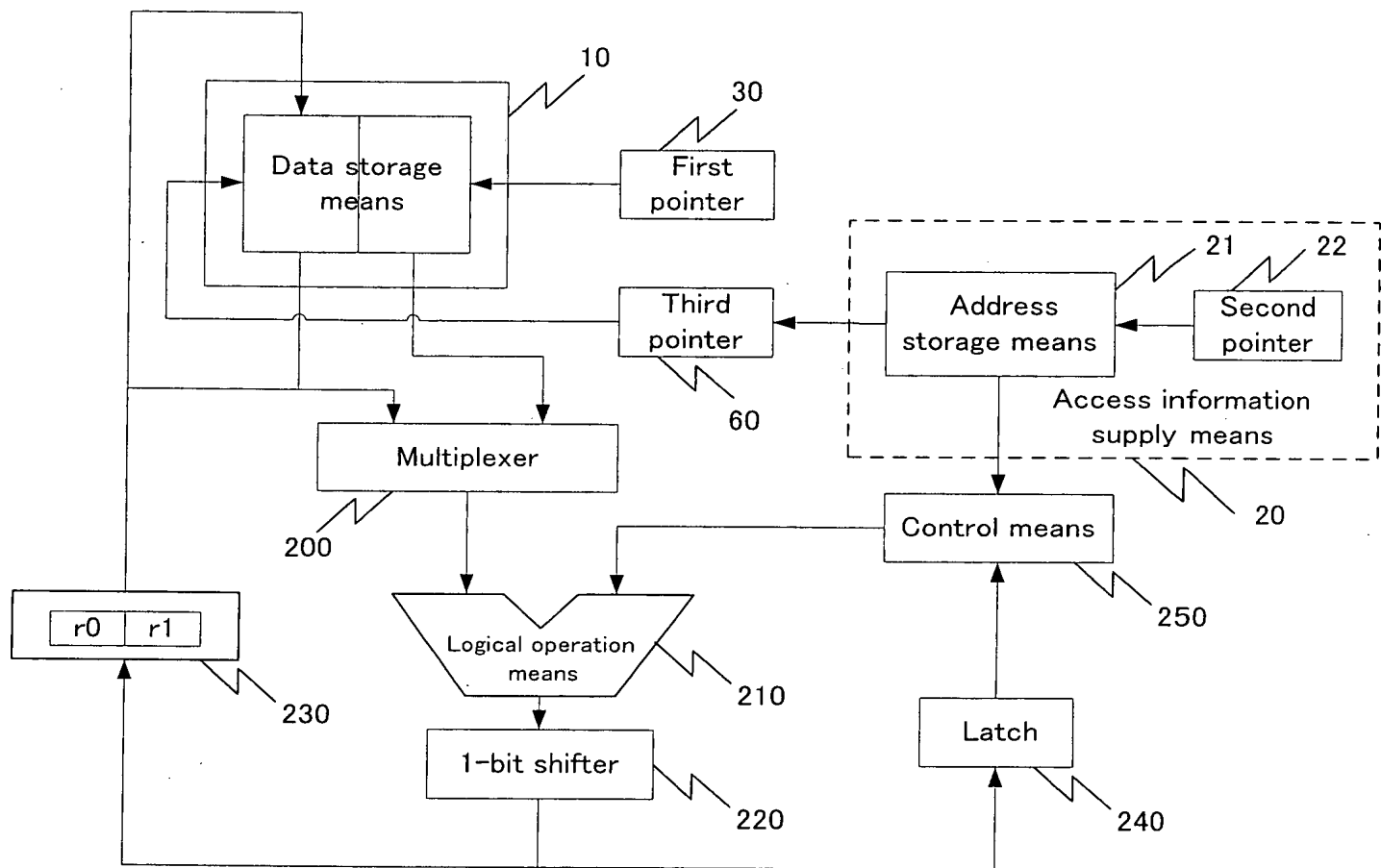
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Date: April 24, 2007
JEL/DWW/att

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FIG. 13
RELATED ART



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FIG. 14

RELATED ART

Step	Processing
step0	Third pointer 60 \leftarrow address information
step1	r1 \leftarrow data storage means 10 (at address designated by first pointer 30) First pointer 30 \leftarrow first pointer 30 + 1
step2	Setting of the number of repetitions
step3	r0 \leftarrow setting of flag of latch 240 in specific bit of 1-word data stored in data storage means 10 (at address designated by third pointer 60) Second pointer 22 \leftarrow second pointer 22 + 1
step4	Data storage means 10 (at address designated by third pointer 60) \leftarrow r0
step5	r1 \leftarrow shifting of data in r1 to higher-order bits by one bit Third pointer 60 \leftarrow address information Return to step 3
step6	Return to step 1